1. [Original] An integrated circuit comprising:

a first circuit branch, coupled between a first node and a second node, comprising a first amplifier stage;

a second circuit branch, coupled between the second node and a third node, comprising a first impedance matching unit and a second amplifier stage, coupled in series; and

a third circuit branch, coupled between the second node and the third node, comprising an impedance transformer unit,

wherein during a first mode of operation of the circuit, the second amplifier stage is in an off state, consuming less power than in an on state, and a signal output from the first amplifier stage passes substantially through the third circuit branch, and

during a second mode of operation of the circuit, the second amplifier stage is in the on state and a signal output from the first amplifier stage passes substantially through the second circuit branch.

2. [Cancelled] The integrated circuit of claim 1 wherein a gain of the first amplifier stage is variable.

3. [Original] The integrated circuit of claim 1 wherein a gain of the first amplifier stage is fixed.

4. [Original] The integrated circuit of claim 1 wherein the first amplifier stage comprises a predistorter circuit.

5. [Original] The integrated circuit of claim 1 wherein the first amplifier stage comprises a gain characteristic to compensate for nonlinearities in a gain characteristic of the second amplifier stage.

6. [Original] The integrated circuit of claim 1 wherein a gain characteristic of the circuit, after passing through both the first amplifier stage and the second amplifier stage, is more linear than the gain characteristic of the second amplifier stage.

7. [Original] The integrated circuit of claim 1 wherein the first circuit branch, second circuit branch, and third circuit branch are formed on a single semiconductor substrate.

8. [Original] The integrated circuit of claim 1 further comprising:

a voltage control circuit coupled to the second amplifier stage, wherein the voltage control circuit, in response to a mode control voltage, provides a signal to the second amplifier stage to place the second amplifier stage in the on state or the off state.

9. [Cancelled] The integrated circuit of claim 1 further comprising:

a voltage control circuit coupled to the first amplifier stage and second amplifier stage,

wherein the voltage control circuit, in response to a mode control voltage, provides a first signal to the first amplifier stage to adjust a bias of the first amplifier stage so during the first mode of operation the bias of the first amplifier stage is reduced compared to the bias of the first amplifier stage during the second mode of operation, and

the voltage control circuit, in response to the mode control voltage, provides a second signal to the second amplifier stage to place the second amplifier stage in the on state or the off state.

10. [Cancelled] The integrated circuit of claim 1 further comprising:

a voltage control circuit coupled to the first amplifier stage and second amplifier stage,

wherein the voltage control circuit, in response to a mode control voltage, provides a first signal to the first amplifier stage to adjust a bias current of the first amplifier stage so during the first mode of operation the bias current of the first amplifier stage is reduced compared to the bias current of the first amplifier stage during the second mode of operation, and

the voltage control circuit, in response to the mode control voltage, provides a second signal to the second amplifier stage to place the second amplifier stage in the on state or the off state.

11. [Original] An integrated circuit comprising:

a first circuit branch, coupled between a first node and a second node, comprising a first amplifier stage and a second amplifier stage, coupled in series;

a second circuit branch, coupled between the second node and a third node, comprising a first impedance matching unit and a third amplifier stage, coupled in series; and

a third circuit branch, coupled between the second node and the third node, comprising an impedance transformer unit,

wherein during a first mode of operation of the circuit, the third amplifier stage is in an off state, consuming less power than in an on state, and a signal output from the first amplifier stage passes through the second amplifier stage and substantially through the third circuit branch, and

during a second mode of operation of the amplifier circuit, the third amplifier stage is in the on state and the signal output from the first amplifier stage passes through the second amplifier stage and substantially through the second circuit branch.

12. [Cancelled] The integrated circuit of claim 11 wherein a gain of the first amplifier stage is variable.

13. [Original] The integrated circuit of claim 11 wherein a gain of the first amplifier stage is fixed.

14. [Original] The integrated circuit of claim 11 wherein the first amplifier stage comprises a predistorter circuit.

15. [Original] The integrated circuit of claim 11 wherein the first amplifier stage comprises a gain characteristic to compensate for nonlinearities in gain characteristics of the second and third amplifier stage.

16. [Original] The integrated circuit of claim 11 wherein a gain characteristic of the circuit, after passing through each of the first amplifier stage, second amplifier stage, and third amplifier stags, is more linear than the gain characteristic of the third amplifier stage.

17. [Original] The integrated circuit of claim 11 wherein the first circuit branch, second circuit branch, and third circuit branch are formed on a single semiconductor substrate.

18. [Original] The integrated circuit of claim 11 further comprising:

a voltage control circuit coupled to the third amplifier stage, wherein the voltage control circuit, in response to a mode control voltage, provides a control signal to the third amplifier stage to place the third amplifier stage in the on state or the off state.

19. [Cancelled] The integrated circuit of claim 11 further comprising:

a voltage control circuit coupled to the first amplifier stage, second amplifier stage, and third amplifier stage, wherein the voltage control circuit, in response to a mode control voltage, provides a first signal to the first amplifier stage or the second amplifier stage to adjust a bias of the first amplifier stage or the second amplifier stage so during the first mode of operation the bias of the first amplifier stage or the second amplifier stage is reduced compared to the bias of the first amplifier stage or the second amplifier stage during the second mode of operation, and

the voltage control circuit, in response to the mode control voltage, provides a second signal to the third amplifier stage to place the third amplifier stage in the on state or the off state.

20. [Cancelled] The integrated circuit of claim 11 further comprising:

a voltage control circuit coupled to each of the first amplifier stage, second amplifier stage, and third amplifier stage,

wherein the voltage control circuit, in response to a mode control voltage, provides a first signal to the first amplifier stage or the second amplifier stage to adjust a bias current of the first amplifier stage or the second amplifier stage so during the first mode of operation the bias current of the first amplifier stage or the second amplifier stage is reduced compared to the bias current of the first amplifier stage or the second amplifier stage during the second mode of operation, and

the voltage control circuit, in response to the mode control voltage, provides a second signal to the third amplifier stage to place the third amplifier stage in the on state or the off state.

21. [Original] An integrated circuit comprising:

a first transistor coupled between an input node and a first node;

a first circuit block coupled between the first node and a second node;

a second circuit block coupled between the second node and a third node;

a second transistor coupled between the third node and a fourth node;

a third circuit block coupled between the fourth node and a fifth node; and

a fourth circuit block coupled between the second node and the fifth node,

wherein in a first mode of operation, a signal provided at the input node passes through the first transistor, first circuit block, and fourth circuit block, and

in a second mode of operation, the signal provided at the input node passes through the first transistor, first circuit block, second circuit block, second transistor, and third circuit block.

22. [Original] The integrated circuit of claim 21 wherein the fourth circuit block comprises:

an inductance device coupled between the second node and a sixth node; and

a capacitor coupled between the sixth node and fifth node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

23. [Original] The integrated circuit of claim 21 wherein the fourth circuit block comprises:

a capacitor coupled between the second node and a sixth node; and

an inductance device coupled between the sixth node and the fifth node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

24. [Original] The integrated circuit of claim 21 wherein the fourth circuit block comprises:

a first capacitor coupled between the second node and a sixth node;

an inductance device coupled between the sixth node and the fifth node; and

a second capacitor coupled between the sixth node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

25. [Original] The integrated circuit of claim 21 wherein the fourth circuit block comprises:

an inductance device coupled between the second node and a sixth node;

a first capacitor coupled between the sixth node and the fifth node; and

a second capacitor coupled between the sixth node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

26. [Original] The integrated circuit of claim 21 wherein the fourth circuit block comprises:

an inductance device coupled between the second node and the fifth node; and

a capacitor coupled between the second node and the fifth node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

27. [Original] The integrated circuit of claim 21 wherein the fourth circuit block comprises:

an inductance device coupled between the second node and the fifth node;

a first capacitor coupled between the second node and a reference voltage level; and

a second capacitor coupled between the fifth node and the reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

28. [Original] The integrated circuit of claim 21 wherein the fourth circuit block comprises:

an inductance device, coupled between the second node and the fifth node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

29. [Original] The integrated circuit of claim 21 wherein the third circuit block comprises:

an inductance device coupled between the fourth node and the fifth node; and

a capacitor coupled between the fourth node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

30. [Original] The integrated circuit of claim 21 wherein the third circuit block comprises:

a first capacitor coupled between the fourth node and a reference voltage level;

a first inductance device coupled between the fourth node and the reference voltage level; and

a second inductance device coupled between the fourth node and the fifth node, wherein the first inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide, and the second inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

31. [Original] The integrated circuit of claim 21 wherein the third circuit block comprises:

a first inductance device coupled between the fourth node and a reference voltage level;

a first capacitor coupled between the fourth node and the reference voltage level;

a second inductance device coupled between the fourth node and the fifth node; and

a second capacitor coupled between the fifth node and the reference voltage level, wherein the first inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide, and the second inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

32. [Original] The integrated circuit of claim 21 wherein the third circuit block comprises:

a first inductance device coupled between the fourth node and a reference voltage level;

a second inductance device coupled between the fourth node and the fifth node; and

a first capacitor coupled between the fifth node and the reference voltage level, wherein the first inductance device comprises at least one of an inductor, wire bonding,

transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide, and the second inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

33. [Original] The integrated circuit of claim 21 wherein the third circuit block comprises:

a first capacitor coupled between the fourth node and a reference voltage level;

a first inductance device coupled between the fourth node and the fifth node; and

a second inductance device coupled between the fifth node and the reference voltage level, wherein the first inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide, and the second inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

34. [Original] The integrated circuit of claim 21 wherein the first circuit block comprises a first capacitor coupled between the first node and a second node, and wherein the second circuit block comprises a second capacitor coupled between the second node and a third node.

35. [Original] The integrated circuit of claim 21 wherein the first circuit block comprises no passive elements coupled between the first node and a second node, and the second circuit block comprises a second capacitor coupled between the second node and a third node.

36. [Original] The integrated circuit of claim 34 wherein the first circuit block further comprises an inductance device and a third capacitor, in series, coupled between the first node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

37. [Original] The integrated circuit of claim 36 wherein the inductance device is further coupled to a supply voltage level.

38. [Original] The integrated circuit of claim 34 wherein the second circuit block further comprises an inductance device coupled between the second node and a reference voltage

level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

39. [Original] The integrated circuit of claim 36 wherein the second circuit block further comprises an inductance device coupled between the second node and the reference voltage level.

40. [Original] The integrated circuit of claim 34 wherein the second circuit block further comprises an inductance device coupled between the third node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

41. [Original] The integrated circuit of claim 34 wherein the second circuit block further comprises a third capacitor coupled between the second node and a reference voltage level.

42. [Original] The integrated circuit of claim 21 wherein the first circuit block comprises an inductance device coupled between the first node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

43. [Original] The integrated circuit of claim 21 wherein the second circuit block comprises:

a first capacitor coupled between the second node and a sixth node;

an inductance device coupled between the sixth node and a reference voltage level; and

a second capacitor coupled between the sixth node and the third node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

44. [Original] The integrated circuit of claim 21 further comprising

a voltage control circuit coupled to the second transistor, wherein the voltage control circuit, in response to a mode control voltage, provides a control signal to the second transistor to place the second transistor in an on state or an off state.

45. [Original] The integrated circuit of claim 44 wherein the voltage control circuit comprises a third transistor coupled between the second transistor and a reference voltage level, wherein an electrode of the third transistor is coupled to a voltage control line.

46. [Original] The integrated circuit of claim 44 wherein the voltage control circuit comprises a third transistor coupled between the second transistor and a reference voltage level and a fourth transistor coupled between a supply voltage line and a reference voltage level, wherein an electrode of the third transistor is connected to the coupled point of the fourth transistor toward the supply voltage line and an electrode of the fourth transistor is coupled to a voltage control line.

47. [Original] The integrated circuit of claim 44 wherein the voltage control circuit comprises a third transistor coupled between the second transistor and a reference voltage level and a fourth transistor coupled between a supply voltage line and an electrode of the third transistor, wherein an electrode of the third transistor is coupled to the fourth transistor and an electrode of the fourth transistor is coupled to a voltage control line.

48. [Cancelled] The integrated circuit of claim 21 further comprising

a voltage control circuit coupled to the first transistor, wherein the voltage control circuit, in response to the mode control voltage, provides a signal to the first transistor to adjust a bias of the first transistor so during the first mode of operation the bias of the first transistor is reduced compared to the bias of the first transistor during the second mode of operation.

49. [Cancelled] The integrated circuit of claim 48 wherein the voltage control circuit comprises a third transistor coupled to the first transistor through a resistance and coupled to a reference voltage level through a resistance, wherein an electrode of the third transistor is coupled to a voltage control line.

50. [Cancelled] The integrated circuit of claim 48 wherein the voltage control circuit comprises a third transistor coupled to the first transistor and coupled to a reference voltage level through a resistance, wherein an electrode of the third transistor is coupled to a voltage control line.

51. [Cancelled] The integrated circuit of claim 48 wherein the voltage control circuit comprises a third transistor coupled to the first transistor through a resistance and coupled to a reference voltage level, wherein an electrode of the third transistor is coupled to a voltage control line.

52. [Cancelled] The integrated circuit of claim 48 wherein the voltage control circuit comprises:

a third transistor;

a resistance; and

one or more level shifting diodes, connected in series with the resistance,

wherein the resistance and the one or more level shifting diodes are coupled in series to the first transistor,

the third transistor is coupled to the resistance and the one or more level shifting diodes and coupled to a reference voltage level, and

an electrode of the third transistor is coupled to a voltage control line.

53. [Original] The integrated circuit of claim 21 wherein the first transistor or the second transistor is a bipolar junction transistor, a heterojunction bipolar transistor, a field effect transistor, a complementary metal-oxide semiconductor transistor, a metal-oxide semiconductor transistor, p-type metal-oxide semiconductor transistor, n-type metal-oxide semiconductor transistor, a high electron mobility transistor, or a metal semiconductor field effect transistor.

54. [Original] An integrated circuit comprising:

a first transistor coupled between an input node and a first node;

a matching circuit block coupled between the first node and a second node;

the second transistor coupled between the second node and a third node;

a first circuit block coupled between the third node and a fourth node;

a second circuit block coupled between the fourth node and a fifth node;

a third transistor coupled between the fifth node and a sixth node;

a third circuit block coupled between the sixth node and a seventh node; and

a fourth circuit block coupled between the fourth node and the seventh node,

wherein in a first mode of operation, a signal provided at the input node passes through the first

transistor, matching circuit block, second transistor, first circuit block, and fourth circuit block, and

in a second mode of operation, a signal provided at the input node passes through the first transistor, matching circuit block, second transistor, first circuit block, second circuit block, third transistor, third circuit block.

55. [Original] The integrated circuit of claim 54 wherein the fourth circuit block comprises:

an inductance device coupled between the fourth node and a eighth node; and

a capacitor coupled between the eighth node and seventh node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

56. [Original] The integrated circuit of claim 54 wherein the fourth circuit block comprises:

a capacitor coupled between the fourth node and a eighth node; and

an inductance device coupled between the eighth node and the seventh node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

57. [Original] The integrated circuit of claim 54 wherein the fourth circuit block comprises:

a first capacitor coupled between the fourth node and a eighth node;

an inductance device coupled between the eighth node and the seventh node; and

a second capacitor coupled between the eighth node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

58. [Original] The integrated circuit of claim 54 wherein the fourth circuit block comprises:

an inductance device coupled between the fourth node and a eighth node;

a first capacitor coupled between the eighth node and the seventh node; and

a second capacitor coupled between the eighth node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

59. [Original] The integrated circuit of claim 54 wherein the fourth circuit block comprises:

an inductance device coupled between the fourth node and the seventh node; and

a capacitor coupled between the fourth node and the seventh node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

60. [Original] The integrated circuit of claim 54 wherein the fourth circuit block comprises:

an inductance device coupled between the fourth node and the seventh node;

a first capacitor coupled between the fourth node and a reference voltage level; and

a second capacitor coupled between the seventh node and the reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

61. [Original] The integrated circuit of claim 54 wherein the fourth circuit block comprises:

an inductance device, coupled between the second node and the fifth node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

62. [Original] The integrated circuit of claim 54 wherein the third circuit block comprises:

an inductance device coupled between the sixth node and the seventh node; and

a capacitor coupled between the sixth node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

63. [Original] The integrated circuit of claim 54 wherein the third circuit block comprises:

a first capacitor coupled between the sixth node and a reference voltage level;

a first inductance device coupled between the sixth node and the reference voltage level; and

a second inductance device coupled between the sixth node and the seventh node, wherein the first inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide, and the second inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

64. [Original] The integrated circuit of claim 54 wherein the third circuit block comprises:

a first inductance device coupled between the sixth node and a reference voltage level;

a first capacitor coupled between the sixth node and the reference voltage level;

a second inductance device coupled between the sixth node and the seventh node; and

a second capacitor coupled between the seventh node and the reference voltage level, wherein the first inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide, and the second inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

65. [Original] The integrated circuit of claim 54 wherein the third circuit block comprises:

a first inductance device coupled between the sixth node and the reference voltage level;

a second inductance device coupled between the sixth node and the seventh node; and

a first capacitor coupled between the seventh node and the reference voltage level, wherein the first inductance device comprises at least one of an inductor, wire bonding,

transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide, and the second inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

66. [Original] The integrated circuit of claim 54 wherein the third circuit block comprises:

a first capacitor coupled between the sixth node and a reference voltage level;

a first inductance device coupled between the sixth node and the seventh node; and

a second inductance device coupled between the seventh node and the reference voltage level, wherein the first inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide, and the second inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

67. [Original] The integrated circuit of claim 54 wherein the first circuit block comprises a first capacitor coupled between the third node and a fourth node, and the second circuit block comprises a second capacitor coupled between the fourth node and a fifth node.

68. [Original] The integrated circuit of claim 54 wherein the first circuit block comprises no passive elements coupled between the third node and a fourth node, and the second circuit block comprises a second capacitor coupled between the fourth node and a fifth node.

69. [Original] The integrated circuit of claim 67 wherein the first circuit block further comprises an inductance device and a third capacitor, in series, coupled between the third node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

70. [Original] The integrated circuit of claim 69 wherein the inductance device is further coupled to a supply voltage level.

71. [Original] The integrated circuit of claim 67 wherein the second circuit block further comprises an inductance device coupled between the fourth node and a reference voltage

level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

72. [Original] The integrated circuit of claim 69 wherein the second circuit block further comprises an inductance device coupled between the fourth node and the reference voltage level.

73. [Original] The integrated circuit of claim 67 wherein the second circuit block further comprises an inductance device coupled between the fifth node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

74. [Original] The integrated circuit of claim 67 wherein the second circuit block further comprises a third capacitor coupled between the fourth node and a reference voltage level.

75. [Original] The integrated circuit of claim 54 wherein the first circuit block comprises an inductance device coupled between the third node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

76. [Original] The integrated circuit of claim 54 wherein the second circuit block comprises:

a first capacitor coupled between the fourth node and a eighth node;

an inductance device coupled between the eighth node and a reference voltage level; and

a second capacitor coupled between the eighth node and the fifth node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

77. [Original] The integrated circuit of claim 54 further comprising;

a voltage control circuit coupled to the third transistor, wherein the voltage control circuit, in response to a mode control voltage, provides a control signal to the third transistor to place the third transistor in the on state or the off state.

78. [Original] The integrated circuit of claim 77 wherein the voltage control circuit comprises a fourth transistor coupled between the third transistor and a reference voltage level, wherein an electrode of the fourth transistor is coupled to a voltage control line.

79. [Original] The integrated circuit of claim 77 wherein the voltage control circuit comprises:

a fourth transistor, coupled between the third transistor and a reference voltage level; and

a fifth transistor, coupled between a supply voltage line and a reference voltage level,

wherein an electrode of the fourth transistor is connected to a point coupling the fifth transistor and the supply voltage line, and

an electrode of the fifth transistor is coupled to a voltage control line.

80. [Original] The integrated circuit of claim 77 wherein the voltage control circuit comprises:

a fourth transistor, coupled between the third transistor and a reference voltage level; and

a fifth transistor, coupled between a supply voltage line and an electrode of the fourth transistor,

wherein an electrode of the fifth transistor is coupled to a voltage control line.

81. [Cancelled] The integrated circuit of claim 54 further comprising

a voltage control circuit coupled to the first transistor or the second transistor, wherein the voltage control circuit, in response to a mode control voltage, provides a signal to the first transistor or the second transistor to adjust a bias of the first transistor or the second transistor so during the first mode of operation the bias of the first transistor or the second transistor is reduced compared to the bias of the first transistor or the second transistor during the second mode of operation.

82. [Cancelled] The integrated circuit of claim 81 wherein the voltage control circuit comprises a fourth transistor coupled to the first transistor or the second transistor through

a resistance and coupled to a reference voltage level through a resistance, wherein an electrode of the fourth transistor is coupled to a voltage control line.

83. [Cancelled] The integrated circuit of claim 81 wherein the voltage control circuit comprises a fourth transistor coupled to the first transistor or the second transistor and coupled to a reference voltage level through a resistance, wherein an electrode of the fourth transistor is coupled to a voltage control line.

84. [Cancelled] The integrated circuit of claim 81 wherein the voltage control circuit comprises a fourth transistor, coupled to the first transistor or the second transistor through a resistance and coupled to a reference voltage level, wherein an electrode of the fourth transistor is coupled to a voltage control line.

85. [Cancelled] The integrated circuit of claim 81 wherein the voltage control circuit comprises:

a fourth transistor;

a resistance; and

one or more level shifting diodes, connected in series with the resistance,

wherein the resistance and the one or more level shifting diodes, in series, are coupled to the first transistor or the second transistor,

the fourth transistor is coupled to the resistance and the one or more level shifting diodes and coupled to a reference voltage level, and

an electrode of the fourth transistor is coupled to a voltage control line.

86. [Original] The integrated circuit of claim 54 wherein the first transistor, second transistor, or third transistor is a bipolar junction transistor, a heterojunction bipolar transistor, a field effect transistor, a complementary metal-oxide semiconductor transistor, a metal-oxide semiconductor transistor, a p-type metal-oxide semiconductor transistor, a n-type metal-oxide semiconductor transistor, a high electron mobility transistor, or a metal semiconductor field effect transistor.

87. [Original] An integrated circuit comprising:

a first circuit branch, coupled between a first node and a second node, comprising N amplifier stages in series, wherein N is an integer 0 or greater,

a second circuit branch, coupled between the second node and a third node, comprising M amplifier stages in series, wherein M is an integer 1 or greater; and

a third circuit branch, coupled between the second node and the third node, comprising an impedance transformer unit,

wherein during a first mode of operation of the circuit, at least one amplifier stage of the M amplifier stages of the second branch is in an off state, consuming less power than in an on state, and a signal output from the N amplifier stages of the first branch passes substantially through the third circuit branch, and

during a second mode of operation of the circuit, the M amplifier stages of the second circuit branch are in the on state and a signal output from N amplifier stages of the first branch passes substantially through the second circuit branch.

88. [Cancelled] The integrated circuit of claim 87 wherein a gain of at least one amplifier stage of the N amplifier stages of the first branch is variable.

89. [Original] The integrated circuit of claim 87 wherein a gain of at least one amplifier stage of the N amplifier stages of the first branch is fixed.

90. [Original] The integrated circuit of claim 87 wherein at least one amplifier stage of the N amplifier stages of the first branch comprises a predistorter circuit.

91. [Original] The integrated circuit of claim 87 wherein at least one amplifier stage of the N amplifier stages of the first branch comprises a gain characteristic to compensate for nonlinearities in a gain characteristic of at least one amplifier stage of M amplifier stages of the second branch.

92. [Original] The integrated circuit of claim 87 wherein a gain characteristic of the circuit, after passing through both the first branch and the second branch, is more linear than the gain characteristic of the second branch.

93. [Original] The integrated circuit of claim 87 wherein the first circuit branch, second circuit branch, and third circuit branch are formed on a single semiconductor substrate.

94. [Original] The integrated circuit of claim 87 further comprising

a voltage control coupled to the least one amplifier stage of the M amplifier stages of the second branch, wherein the voltage control circuit, in response to a mode control voltage, provides a control signal to the least one amplifier stage of the M amplifier stages of the second branch to place the least one amplifier stage of the M amplifier stages of the second branch in an on state or an off state.

95. [Cancelled] The integrated circuit of claim 87 further comprising:

a voltage control circuit coupled to at least one amplifier stage of the N amplifier stages of the first branch and the at least one amplifier stage of the M amplifier stages of the second branch,

wherein the voltage control circuit, in response to a mode control voltage, provides a first signal to the at least one amplifier stage of the N amplifier stages of the first branch to adjust a bias of the at least one amplifier stage of the N amplifier stages of the first branch so during the first mode of operation the bias of the at least one amplifier stage of the N amplifier stages of the first branch is reduced compared to the bias of the at least one amplifier stage of the N amplifier stages of the first branch during the second mode of operation, and

the voltage control circuit, in response to the mode control voltage, provides a second signal to the at least one amplifier stage of the M amplifier stages of the second branch to place the at least one amplifier stage of the M amplifier stages of the second branch in the on state or the off state.

96. [Cancelled] The integrated circuit of claim 87 further comprising:

a voltage control circuit coupled to at least one amplifier stage of the N amplifier stages of the first branch and the at least one amplifier stage of the M amplifier stages of the second branch,

wherein the voltage control circuit, in response to a mode control voltage, provides a first signal to the at least one amplifier stage of the N amplifier stages of the first branch to adjust a bias current of the at least one amplifier stage of the N amplifier stages of the first branch so during the first mode of operation the bias current of the at least one amplifier stage of the N amplifier stages of the first branch is reduced compared to the bias current of the

at least one amplifier stage of the N amplifier stages of the first branch during the second mode of operation, and

the voltage control circuit, in response to the mode control voltage, provides a second signal to the at least one amplifier stage of the M amplifier stages of the second branch to place the at least one amplifier stage of the M amplifier stages of the second branch in the on state or the off state.

97. [Original] The integrated circuit of claim 94 wherein the voltage control circuit comprises a transistor coupled between the least one amplifier stage of the M amplifier stages of the second branch and a reference voltage level, wherein an electrode of the transistor is coupled to a voltage control line.

98. [Original] The integrated circuit of claim 94 wherein the voltage control circuit comprises a transistor coupled between the least one amplifier stage of the M amplifier stages of the second branch and a reference voltage level and another transistor coupled between a supply voltage line and a reference voltage level, wherein an electrode of the former transistor is connected to the coupled point of the latter transistor toward the supply voltage line and an electrode of the latter transistor is coupled to a voltage control line.

99. [Original] The integrated circuit of claim 94 wherein the voltage control circuit comprises a transistor coupled between the least one amplifier stage of the M amplifier stages of the second branch and a reference voltage level and another transistor coupled between a supply voltage line and an electrode of the former transistor, wherein an electrode of the former transistor is coupled to the latter transistor and an electrode of the latter transistor is coupled to a voltage control line.

100. [Cancelled] The integrated circuit of claim 87 further comprising

a voltage control circuit coupled to the least one amplifier stage of the N amplifier stages of the first branch, wherein the voltage control circuit, in response to the mode control voltage, provides a signal to the least one amplifier stage of the N amplifier stages of the first branch to adjust a bias of the least one amplifier stage of the N amplifier stages of the first branch so during the first mode of operation the bias of the least one amplifier stage of the N

amplifier stages of the first branch is reduced compared to the bias of the least one amplifier stage of the N amplifier stages of the first branch during the second mode of operation.

101. [Cancelled] The integrated circuit of claim 100 wherein the voltage control circuit comprises a transistor coupled to the least one amplifier stage of the N amplifier stages of the first branch through a resistance and coupled to a reference voltage level through a resistance, wherein an electrode of the third transistor is coupled to a voltage control line.

102. [Cancelled] The integrated circuit of claim 100 wherein the voltage control circuit comprises a transistor coupled to the least one amplifier stage of the N amplifier stages of the first branch and coupled to a reference voltage level through a resistance, wherein an electrode of the transistor is coupled to a voltage control line.

103. [Cancelled] The integrated circuit of claim 100 wherein the voltage control circuit comprises a transistor coupled to the least one amplifier stage of the N amplifier stages of the first branch through a resistance and coupled to a reference voltage level, wherein an electrode of the transistor is coupled to a voltage control line.

104. [Cancelled] The integrated circuit of claim 100 wherein the voltage control circuit comprises:

a transistor;

a resistance; and

one or more level shifting diodes, connected in series with the resistance,

wherein the resistance and the one or more level shifting diodes are coupled in series to the least one amplifier stage of the N amplifier stages of the first branch,

the transistor is coupled to the resistance and the one or more level shifting diodes and coupled to a reference voltage level, and

an electrode of the transistor is coupled to a voltage control line

105. [Original] The integrated circuit of claim 1 wherein the integrated circuit contains no bypass switches, wherein switches may include any of a relay, micromachined switch, transistor switch, PIN diode switch, or Schottky diode switch.

106. [Original] The integrated circuit of claim 1 wherein the first branch, second branch and third branch contain no bypass switches, wherein switches may include any of a relay, micromachined switch, transistor switch, PIN diode switch, or Schottky diode switch.

107. [Original] The integrated circuit of claim 11 wherein the integrated circuit contains no bypass switches, wherein switches may include any of a relay, micromachined switch, transistor switch, PIN diode switch, or Schottky diode switch.

108. [Original] The integrated circuit of claim 11 wherein the first branch, second branch and third branch contain no bypass switches, wherein switches may include any of a relay, micromachined switch, transistor switch, PIN diode switch, or Schottky diode switch.

109. [Original] The integrated circuit of claim 87 wherein the integrated circuit contains no bypass switches, wherein switches may include any of a relay, micromachined switch, transistor switch, PIN diode switch, or Schottky diode switch.

110. [Original] The integrated circuit of claim 87 wherein the first branch, second branch and third branch contain no bypass switches, wherein switches may include any of a relay, micromachined switch, transistor switch, PIN diode switch, or Schottky diode switch.

111. [Original] The integrated circuit of claim 21 further comprising a fifth circuit block coupled between the fifth node and a sixth node.

112. [Original] The integrated circuit of claim 111 wherein the fifth circuit block comprises a capacitor coupled between the fifth node and sixth node.

113. [Original] The integrated circuit of claim 111 wherein the fifth circuit block comprises:

an inductance device coupled between the fifth node and sixth node; and

a capacitor coupled between the sixth node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

114. [Original] The integrated circuit of claim 111 wherein the fifth circuit block comprises:

an inductance device coupled between the fifth node and seventh node;

a first capacitor coupled between the seventh node and a reference voltage level; and

a second capacitor coupled between the seventh node and the sixth node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

115. [Original] The integrated circuit of claim 111 wherein the fifth circuit block comprises an inductance device and capacitor, in series, coupled between the fifth node and sixth node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

116. [Original] The integrated circuit of claim 111 wherein the fifth circuit block comprises:

a first capacitor coupled between the fifth node and a reference voltage level;

an inductance device coupled between the fifth node and sixth node; and

a second capacitor coupled between the sixth node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

117. [Original] The integrated circuit of claim 111 wherein the fifth circuit block comprises:

a capacitor coupled between the fifth node and a reference voltage level;

an inductance device coupled between the fifth node and sixth node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

118. [Original] The integrated circuit of claim 54 further comprising a fifth circuit block coupled between the seventh node and a eighth node.

119. [Original] The integrated circuit of claim 118 wherein the fifth circuit block comprises a capacitor coupled between the seventh node and eighth node.

120. [Original] The integrated circuit of claim 118 wherein the fifth circuit block comprises:

an inductance device coupled between the seventh node and eighth node; and

a capacitor coupled between the eighth node and a reference voltage level,

wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

121. [Original] The integrated circuit of claim 118 wherein the fifth circuit block comprises:

an inductance device coupled between the seventh node and ninth node;

a first capacitor coupled between the ninth node and a reference voltage level; and

a second capacitor coupled between the ninth node and the eighth node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

122. [Original] The integrated circuit of claim 118 wherein the fifth circuit block comprises an inductance device and capacitor, in series, coupled between the seventh node and eighth node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

123. [Original] The integrated circuit of claim 118 wherein the fifth circuit block comprises:

a first capacitor coupled between the seventh node and a reference voltage level;

an inductance device coupled between the seventh node and eighth node; and

a second capacitor coupled between the eighth node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

124. [Original] The integrated circuit of claim 118 wherein the fifth circuit block comprises:

a capacitor coupled between the seventh node and a reference voltage level;

an inductance device coupled between the seventh node and eighth node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

705 125. [Original] The integrated circuit of claim 87 wherein N is 0, 1, 2, 3, 4, or 5.

126. [Cancelled] The integrated circuit of claim 87 wherein M is 2, 3, 4, or 5.

127. [Cancelled] The integrated circuit of claim 87 wherein N is 0, 1, 2, 3, 4, or 5, and M is 2, 3, 4, or 5.